

DSP for FPGAs

SYLLABUS

Introduction to DSP FPGA Hardware

- From discrete logic to FPGAs -some history!
- The generic DSP system
- DSP cores and processors review
- Custom and semi-custom ASICs
- System-on-chip (SOC)
- FPGA flexibility and functionality
- FPGAs vs Programmable DSPs

Linear Systems DSP Algorithm Review

- Aliasing and reconstruction filters
- Sampling rates and wordlengths
- Z-domain notation and fundamental analysis
- Frequency domain analysis
- Finite Impulse Response (FIR) filters
- Infinite Impulse Response (IIR) filters
- Digital filter design and specification
- Oversampling techniques (sigma delta)

FPGA Technology

- The FPGA technology roadmap
- Clocking rates, data rates and sample rates
- FPGA memory and registers
- Input/output blocks and requirements
- Bits, Slices and Configurable Logic Blocks
- Comparable MIPs Performance Ratings
- FPGA Families and Sources

FPGA elements for DSP algorithms

- Building delay lines and Shift Registers
- Use of RAM (memory) on FPGAs
- Serial to Parallel and Parallel to serial
- Multiplexors for channel selection
- Full adders, carry logic, and adder trees
- Multipliers: Shift and Add; ROM based
- Efficient multiplier implementation

DSP Arithmetic Essentials

- 2's complement fixed point arithmetic
- Fundamental adders and multiplier arrays
- Division and square root arrays....not so easy!
- Wordlength issues & Fixed point arithmetic
- Saturate and wraparound
- Overflow and underflow
- CORDIC techniques
- Complex arithmetic requirements

Signal Flow Graph (SFG) Techniques

- DSP/Digital Filter Signal Flow Graphs
- Latency, delays and "anti-delays"!
- Re-timing: Cut-set and delay scaling
- The transpose FIR
- Pipelining and multichannel architectures
- SFG topologies for FPGAs

Frequency Domain Processing

- Discrete Fourier Transform (DFT) Review
- Fast Fourier Transform (FFT)
- The FFT and IFFT
- FFT FPGA architectures
- FFT wordlength growth and accuracy

Digital Filtering for FPGAs

- Symmetric / Linear Phase Filters
- Upsampling and interpolation filters
- Downsampling and decimation filters
- Efficient arithmetic for FIR implementation
- Integrators and differentiators
- Half-band, moving average and comb filters
- Cascade Integrator Comb (CIC) Filters (Hogenauer)
- Efficient arithmetic for IIR Filtering

Adaptive DSP Algorithms and Applications

- Adaptive applications (equalisation, beamforming)
- LMS Algorithms and parallel implementation
- Non-canonical LMS algorithms
- Linear algebra; solving linear systems of equations
- The QR algorithm for adaptive signal processing
- QR processing requirements and numerical issues

DSP Enabled Communications & FPGAs

- Quaternary Phase Shift Keying (QPSK)
- Transmit/Receive Filters - Root Raised Cosine
- Undersampling & Digital Downconversion
- Direct digital upconversion
- Digital IF stages (and fs/4 Systems)
- Numerically controlled oscillators (NCO)
- Channel coding requirements
- Design partitioning for FPGAs

Timing and Synchronisation Issues

- Carrier recovery, squaring & Costas loops, PLLs
- Phase rotations; Sampling rate conversions
- Symbol timing recovery, early/late gate detection
- Multirate and polyphase filters
- Delay locked loop timing and synchronisation

Embedded Processors for FPGAs

- Embedded systems
- System-on-chip design methodologies & flows
- On-chip network topologies and standards
- System profiling and hardware acceleration
- Xilinx Platform Studio (XPS)
- PicoBlaze, MicroBlaze embedded processors
- DSP algorithms on embedded processors

LABORATORY SESSIONS

The laboratory sessions for this course will be based upon the Xilinx DSP design flows. System Generator for Matlab/Simulink, Xilinx ISE and XPS software tools will be used to design DSP systems for the Xilinx XUP development kit.